WHAT IS CLAIMED IS:

1	1. A content processing unit for protecting interchip content pathways
2	transporting digital content objects, the content processing unit comprising:
3	a first chip package, wherein the first chip package comprises:
4	a first body,
5	a first plurality of interconnects,
6	an encryption engine, and
7	a first key storage register capable of storing a first key,
8	wherein:
9	the first key is used by the encryption engine to
10	produce ciphertext content,
1	the first key storage register is non-readable
12	from outside the first body, and
13	the first key storage register cannot be
14	overwritten after a programmability period;
15	a second chip package, wherein the second chip package comprises:
16	a second body,
17	a second plurality of interconnects,
18	a decryption engine, and
19	a second key storage register capable of storing a second key,
20	wherein:
21	the second key is used by the decryption engine
22	to produce plaintext content from the ciphertext content, and
23	the second key storage register is non-readable
24	from outside the second body;
25	a content pathway coupling a first subset of the first plurality and a second
26	subset of the second plurality, wherein the content pathway transports the digital content
27	objects as the ciphertext content.
1	2. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 1, wherein the programmability period
3	ends when a command is sent to the first plurality.

1	 The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 2, wherein the command activates a
3	fusable link.
1	4. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 1, wherein the programmability perio
3	ends after writing to the first key storage register.
1	5. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 1, wherein:
3	the content processing unit is a set top box, and
4	the first chip package is a conditional access chip.
1	6. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 1, wherein at least one of the first and
3	second chip packages comprises a plurality of semiconductor substrates.
1	7. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 1, wherein:
3	at least one of the first and second chip packages further comprises a key
4	encryption key, and
5	at least one of the first and second keys is protected with the key encryption
6	key outside the first body.
1	8. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 1, wherein the second key storage
3	register is overwritable by manipulating the second plurality.
1	9. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 1, wherein:
3	the second chip package further comprises a second encryption engine, and
4	the second encryption engine uses the second key or another key that is a
5	function of the second key to encrypt the content object or a derivative thereof.
1	10. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 9, further comprising a third chip

4	encryption engine.
1	11. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 1, wherein:
3	the content processing unit is part of a larger system comprising a third
4	plurality of functionally equivalent content processing units, and
5	each of the third plurality uses a different first key to protect their respective
6	content pathways.
1	12. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 1, wherein the digital content objects
3	are either compressed or non-compressed.
1	13. A method for protecting interchip content pathways transporting digital
2	content objects within a content processing unit, the method comprising steps of:
3	loading a first key into a first key storage register in a first chip package,
4	wherein the first key in the first key storage register is non-readable from outside the first
5	chip package;
6	activating a feature of the first chip package that prevents overwriting the first
7	key in the first key storage register from outside the first chip package;
8	encrypting digital content with the first key to produce ciphertext content;
9	coupling the ciphertext content from the first chip package to a content
10	pathway;
11	loading a second key into a second key storage register in a second chip
12	package, wherein the second key in the second key storage register is non-readable from
13	outside the second chip package;
14	coupling the ciphertext content from the content pathway to a second chip
15	package; and
16	decrypting the ciphertext content with the second key to reformulate the
17	digital content.
1	14. The method for protecting interchip content pathways transporting
2	digital content objects within the content processing unit as recited in claim 13, further
3	comprising steps of:

package comprising a third key that can decrypt ciphertext produced with the second

4	providing a key encryption key in the at least one of the first and second chip
5	packages; and
6	decrypting at least one of the first and second keys with the key encryption
7	key, whereby the at least one of the first and second keys is protected with the key encryption
8	key outside the first chip package.
1	16 The most ad few must esting interesting content not by your transporting
1	15. The method for protecting interchip content pathways transporting digital content objects within the content processing unit as recited in claim 13, further
2	
3	comprising a step of overwriting the second key in the second key storage register from
4	outside the second chip package.
1	16. The method for protecting interchip content pathways transporting
2	digital content objects within the content processing unit as recited in claim 13, further
3	comprising steps of:
4	encrypting the digital content or a derivative thereof in the second chip
5	package to produce second ciphertext content using the second key or another key that is a
6	function of the second key,
7	coupling the second ciphertext content to a second content pathway.
1	17. The method for protecting interchip content pathways transporting
2	digital content objects within the content processing unit as recited in claim 16, further
3	comprising steps of:
4	coupling the second ciphertext content from the second content pathway to a
5	third chip package; and
	decrypting the second ciphertext content with the third key to reformulate the
6	
7	digital content.
1	18. The method for protecting interchip content pathways transporting
2	digital content objects within the content processing unit as recited in claim 13, wherein:
3	the content processing unit is part of a larger system comprising a plurality of
4	functionally equivalent content processing units, and
5	each of the plurality uses a different first key to protect their respective content
6	pathways.

I	19. The method for protecting interemp content pathways transporting
2	digital content objects within the content processing unit as recited in claim 13, further
3	comprising steps of:
4	replacing at least one of the first and second chip packages;
5	querying a database for at least one of the first and second keys; and
6	loading at least one first and second keys into its respective chip package.
1	20. The method for protecting interchip content pathways transporting
2	digital content objects within the content processing unit as recited in claim 13, further
3	comprising steps of:
4	replacing at least one of the first and second chip packages; and
5	activating a secure re-start feature to load at least one of the first and second
6	keys into its respective chip package from another chip package.
1	21. A computer system adapted to perform the computer-implementable
2	method for protecting interchip content pathways transporting digital content objects within
3	the content processing unit of claim 13.
1	22. A computer-readable medium having computer-executable instructions
2	for performing the computer-implementable method for protecting interchip content
3	pathways transporting digital content objects within the content processing unit of claim 13.
1	23. A content processing unit for protecting interchip content pathways
2	transporting digital content objects, the content processing unit comprising:
3	a first chip package, wherein the first chip package comprises:
4	a first body,
5	a first plurality of interconnects,
6	an encryption engine, and
7	a first key storage register capable of storing a first key,
8	wherein:
9	the first key is used by the encryption engine to
10	produce ciphertext content,
11	the first key storage register is non-readable
12	from the first plurality of interconnects, and

13	the first key storage register cannot be
14	overwritten after being written once;
15	a second chip package, wherein the second chip package comprises:
16	a second body,
17	a second plurality of interconnects,
18	a decryption engine, and
19	a second key storage register capable of storing a second key,
20	wherein:
21	the second key is used by the decryption engine
22	to produce plaintext content from the ciphertext content, and
23	the second key storage register is non-readable
24	from the second plurality of interconnects;
25	a content pathway coupling a first subset of the first plurality and a second
26	subset of the second plurality, wherein the content pathway transports the digital content
27	objects as the ciphertext content.
1	24. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 23, wherein:
3	the first key storage register has a third plurality of bits, and
4	each of the third plurality can only change its stored value, at most, one time.
1	25. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 23, wherein:
3	at least one of the first and second chip packages further comprises a key
4	encryption key, and
5	at least one of the first and second keys is protected with the key encryption
6	key outside the first body.
1	26. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 23, wherein the second key storage
3	register is overwritable from outside the second chip package.
1	27. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 23, wherein:
3	the second chip package further comprises a second encryption engine, and

4	the second encryption engine uses the second key or another key that is a
5	function of the second key to encrypt the content object or a derivative thereof.
1	28. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 27, further comprising a third chip
3	package comprising a third key that can decrypt ciphertext produced with the second
4	encryption engine.
1	29. The content processing unit for protecting interchip content pathways
2	transporting digital content objects as recited in claim 23, wherein:
3	the content processing unit is part of a larger system comprising a third
4	plurality of functionally equivalent content processing units, and
5	each of the third plurality uses a different first key to protect their respective
6	content pathways.